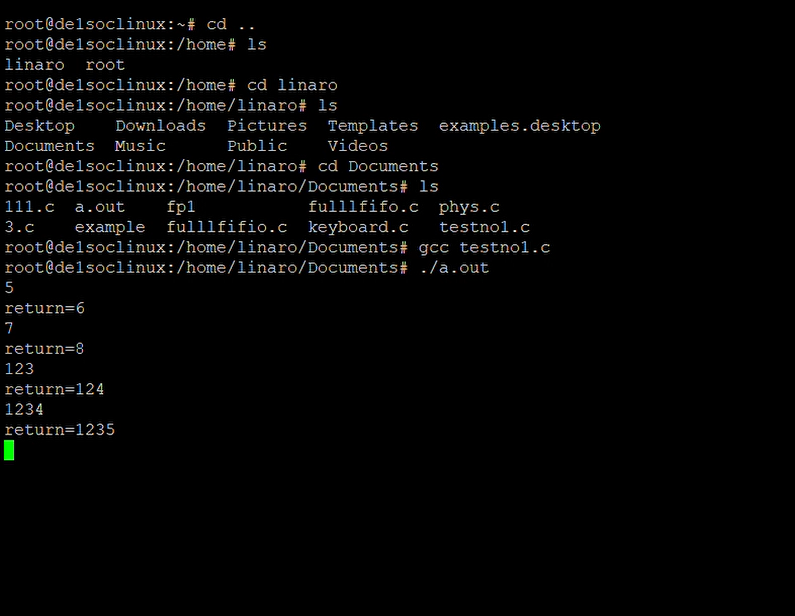
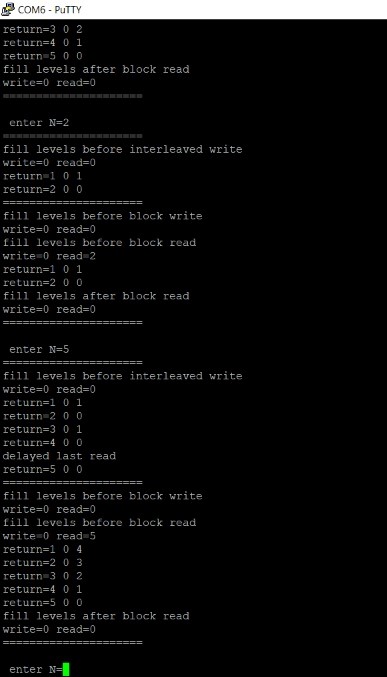
# RESULTS & APPLICATIONS

# OBSERVATIONS :

1. HPS to FPGA FIFO with feedback via SRAM scratchpad.



1. Full FIFO communication: HPS-to-FPGA and FPGA-to-HPS.



# APPLICATIONS :

* Crossing clock domains
* Buffering data before sending it off chip (e.g. To SRAM)
* Buffering data for software to look at some later time
* Storing data for later processing